WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor region of first conductivity formed over a semiconductor substrate of said first conductivity;

a semiconductor trench receiving region formed over said semiconductor region of said first conductivity;

a plurality of trenches formed in said trench receiving region, each trench including a bottom surface and opposing sidewalls;

a channel region of a second conductivity adjacent said trenches;

a conductive column of said first conductivity formed between the bottom surface of each trench and said semiconductor region of said first conductivity;

a charge-balanced region of said second conductivity formed adjacent each conductive column and adjacent said channel region;

conductive regions of said first conductivity formed adjacent each trench and in said channel region;

a gate insulation layer formed at least on said sidewalls of said trenches;

a gate electrode formed in each of said trenches; and

an electrical contact layer formed over said trench receiving region and in contact with said conductive regions of said first conductivity.

2. A semiconductor device according to claim 1, wherein said semiconductor trench receiving region comprises an epitaxial layer of said second conductivity.

3. A semiconductor device according to claim 1, further comprising another electrical contact layer formed over said semiconductor substrate.

4. A semiconductor device according to claim 1, further comprising high conductivity contact regions of said second conductivity type formed in said trench receiving region in electrical contact with said electrical contact layer.

5. A semiconductor device according to claim 1, wherein each of said conductive columns extends above said bottom of a respective trench along its sidewalls.

6. A semiconductor device according to claim 1, wherein said conductive regions of said first conductivity are source regions.

7. A semiconductor device according to claim 1, wherein said epitaxial layer of said first conductivity is a drain region.

8. A semiconductor device comprising:

an epitaxially formed drain region of a first conductivity formed over a semiconductor substrate of the same conductivity;

a trench receiving region;

a plurality of trenches formed in said trench receiving region, each trench including a bottom surface and opposing sidewalls;

a channel region of a second conductivity adjacent said trenches;

source regions of a first conductivity formed in said trench receiving region adjacent said trenches;

a plurality of columns of said first conductivity each formed directly below a respective trench and extending between the bottom of said trench to said drain

region, each column being spaced from another column by a charge-balanced region of said second conductivity;

a gate insulation layer formed at least on said sidewalls of said trenches;

a gate electrode formed in each of said trenches; and

a source contact layer formed over said trench receiving region and in contact with said source regions.

9. A semiconductor device according to claim 8, further comprising another electrical contact layer formed over said semiconductor substrate.

10. A semiconductor device according to claim 8, wherein said charge-balanced regions extend between said channel region and said drain region.

11. A semiconductor device according to claim 8, further comprising high conductivity contact regions of said second conductivity type formed in said trench receiving region in electrical contact with said source contact layer.

12. A semiconductor device according to claim 8, wherein said gate electrodes are comprised of conductive polysilicon.

13. A method for manufacturing a semiconductor device comprising:

providing a trench receiving semiconductor layer of a first conductivity;

forming a mask over said trench receiving semiconductor layer, said mask including openings, each opening terminating at said trench receiving semiconductor layer at its bottom;

forming a trench in said trench receiving layer at said bottom of each of said openings in said mask;

leaving said mask in place;

sequentially implanting dopants of said second conductivity through the bottom of said trench at a plurality of different depths to form a plurality of implant regions below the bottom of said trench;

forming a column of said second conductivity below said trench by applying a diffusion drive so that dopants at each of said plurality of implant regions diffuses to reach at least the dopants of an adjacent implant region.

14. A method according to claim 13, wherein said trench receiving layer is formed over an epitaxial layer of said second conductivity and wherein said dopants at said plurality of said depths join up to form a column that extends between said epitaxial layer and said bottom of said trench.

15. A method according to claim 14, wherein said epitaxial layer is a drain region formed over a substrate of the same conductivity.

16. A method according to claim 13, further comprising forming charge-balanced regions of said first conductivity adjacent said column of said second conductivity.

17. A method according to claim 13, further comprising forming a semiconductor layer below said trench receiving layer, said semiconductor layer including regions of said second conductivity and spaced columns of said first conductivity, and aligning said trenches with said columns of said first conductivity.